

SiPM Evaluation Board Signal amplifier



Features

- Transimpedance SiPM Signal Amplifier
- Low Gain Output
- High Gain Output
- For RGB and NUV AdvanSiD SiPMs
- Suitable for both CSP and TO packaged SiPMs

Applications

- Dark characterization
- CW and Pulsed-Mode measurements
- Photon Detection efficiency measurements
- SPTR measurements
- For laboratory use only

Description

AdvanSiD ASD-EP-N is an evaluation board for RGB and NUV AdvanSiD SiPMs that allows for an easy interface to acquisition systems for optical and electrical device evaluation and testing.

The board has been specifically designed to match and optimize the performances of AdvanSiD SiPMs. It represents the most suitable and reliable way to start using AdvanSiD detectors and it can be used in laboratory environments for dark/light device characterization, low-light measurements, product prototyping.

The ASD-EP-EB-N Evaluation Board is based on a high-gain inverting transimpedance amplifier stage ($Z = 1000 \Omega$) followed by two independent output stages. OUT 1 provides a buffered output with a total transimpedance gain $G1 = 500 \Omega$ when terminated on a 50Ω load. OUT 2 provides a further non-inverting amplification stage with a gain of 5 that gives a total transimpedance gain $G2 = 2500 \Omega$ when terminated on a 50Ω load.

Ordering information

ASD-EP-EB-N Evaluation board with two outputs (low gain, high gain). Negative output signals.

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_A	Supply Voltage Range ($V_{DD} - V_{SS}$)	4.5	12	V
S_{IN}	Common Mode Input Voltage	$V_{SS} - 0.7$	$V_{DD} + 0.7$	V
T_A	Operating Temperature Range	-20	+60	°C
T_S	Storage Temperature	-10	+80	°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

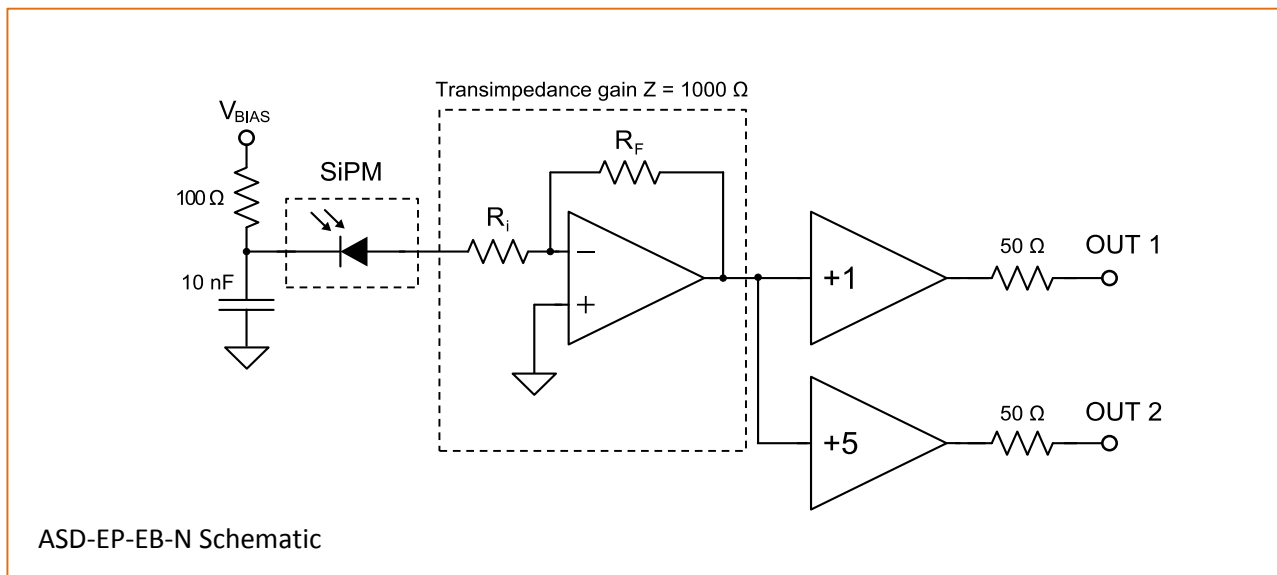
ASD-EP-EB-N Specifications

At $T_A = 25^\circ\text{C}$, $V_{DD} = +5\text{ V}$, $V_{SS} = -5\text{ V}$

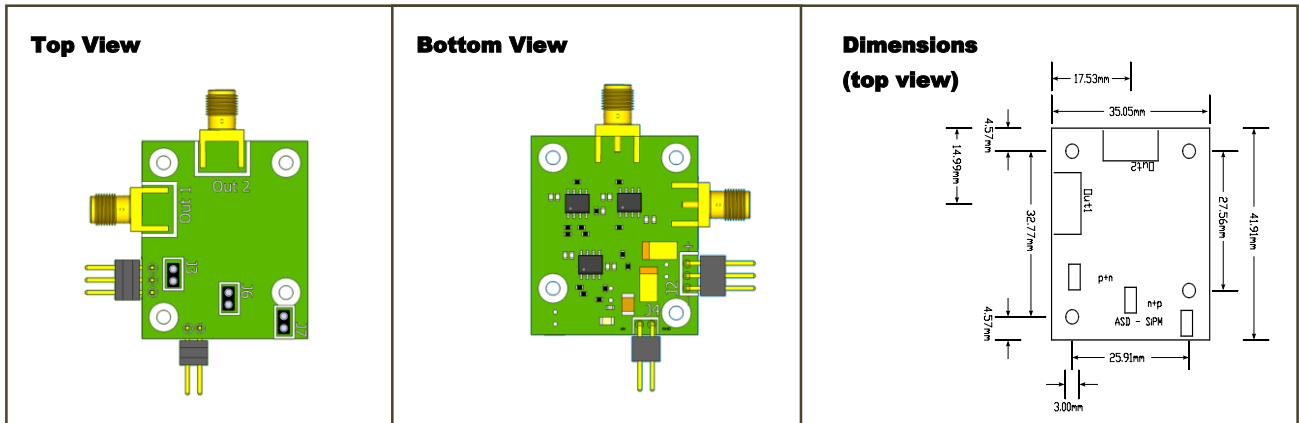
Symbol	Parameter	Value	Unit
Z	Inverting Stage Transimpedance Gain	1000	Ω
G_1	OUT 1 Total Transimpedance ⁽¹⁾	500	Ω
G_2	OUT 2 Total Transimpedance ⁽¹⁾	2500	Ω
Z_{OUT}	Output Impedance ⁽²⁾	50	Ω
I_{SS}	Supply Current	(typ.) 50	mA

(1) Including Z and terminated on $50\ \Omega$ load.

Block Diagram



Layout and dimensions



SiPM connections

The J6 pin header, located on the front side of the Evaluation Board, receives the anode and cathode terminals of the SiPM to be tested.

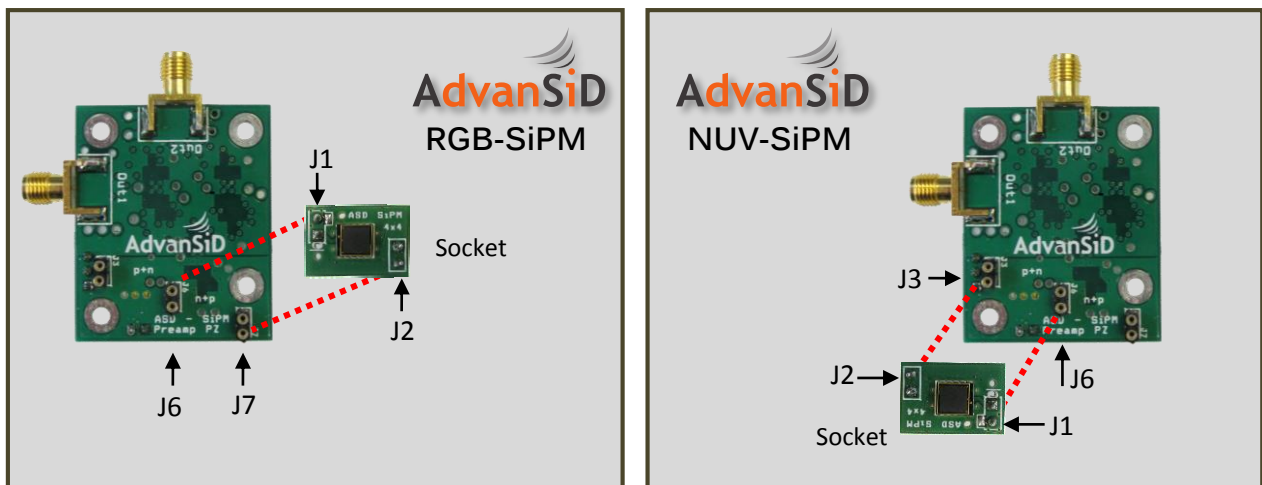
SiPMs in metal can (TO package)

The pins of metal cans can be directly inserted into J6, according to the pin-out reported on the SiPM datasheet and the Evaluation board pin-out scheme reported in this datasheet.

CSP SiPMs

CSP SiPMs connect to the evaluation board through the **AdvanSiD SiPM Sockets** available for 1x1, 3x3, 4x4 mm² RGB and NUV CSP SiPMs.

The SiPM Sockets insert into the AdvanSiD Evaluation Board according to the SiPM type that is carried:
 Sockets with **RGB-SiPM**: J1 (Socket) into J6 (Evaluation Board); J2 (Socket) into J7 (Evaluation Board).
 Sockets with **NUV-SiPM**: J1 (Socket) into J6 (Evaluation Board); J2 (Socket) into J3 (Evaluation Board).



Pin header J3 and J7 are not electrically active; they serve as mechanical support for the socket.

Pin-out

A. Amplifier Power Supply (dual power supply required)

Connector J2:

Pin 1: V_{SS}

Pin 2: GND

Pin 3: V_{DD}

Typical configuration:

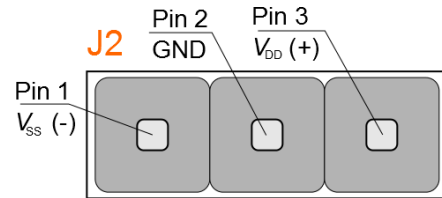
$V_{DD} = +5\text{ V}$

$V_{SS} = -5\text{ V}$

Recommendations:

$(V_{DD} - V_{SS}) = 10\text{ V}$

Power supply capability: $>100\text{ mA}$



B. SiPM Power Supply (for SiPM biasing)

Connector J4:

Pin 1 = V_{BIAS}

Pin 2 = GND

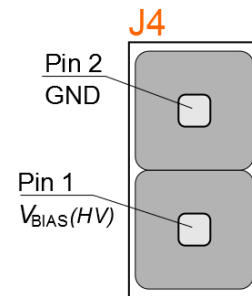
Refer to the SiPM datasheet for the specific device breakdown voltage.

Example:

$|V_{BREAKDOWN}| = 28\text{ V}$ (from SiPM datasheet)

$V_{OVERVOLTAGE} = 4\text{ V}$ (AdvanSiD SiPMs operate with 2 to 7 V overvoltage)

→ $V_{BIAS} = +32\text{ V}$ (Since it is applied in reverse mode, V_{BIAS} must be positive)



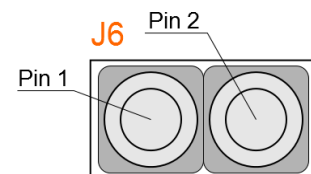
C. Input signal (SiPM anode and cathode)

Socket J6:

Pin 1 = SiPM Anode

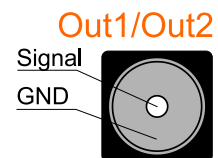
Pin 2 = SiPM Cathode

Note: Socket J6 can host metallic TO packages or the AdvanSiD socket. Refer to the specific device datasheet for SiPM pin-out.



D. Output

SMA connectors



Note: Out1 and Out2 should be terminated with $50\ \Omega$ load for output impedance matching.