AdvanSiD
Advanced Silicon Detectors

ASD-EP-EB-PZ

SiPM Evaluation Board

Signal amplifier

Pole-Zero Compensation

Features

- **Transimpedance SiPM Signal Amplifier**
- **Low Gain Output**
- **Differential Output (Pole-Zero Compensation)**
- **For RGB and NUV AdvanSiD SiPMs**
- **Suitable for both CSP and TO packaged SiPMs**

Applications

- **Energy and Timing measurements (SiPMs with scintillators)**
- **Photon Detection efficiency measurements**
- **SPTR measurements**
- **For laboratory use only**

Description

AdvanSiD ASD-EP-PZ is an evaluation board for RGB and NUV AdvanSiD SiPMs that allows for an easy interface to acquisition systems for optical and electrical device evaluation and testing.

The board has been specifically designed to match and optimize the performances of AdvanSiD SiPMs. It represents the most suitable and reliable way to start using AdvanSiD detectors and it can be used in laboratory environments for dark/light device characterization, low-light measurements, product prototyping.

The ASD-EP-EB-PZ Evaluation Board is based on a low-gain non inverting transimpedance amplifier stage (Z=100 Ω) followed by two independent output stages (OUT 1, OUT 2). OUT 1 provides a buffered output with a total transimpedance gain G1 = 50 Ω when terminated on a 50 Ω load. OUT 2 implements a Pole-Zero (PZ) compensation network followed by an inverting buffer that provides the differentiated version of the SiPM signal. OUT 2 does not preserve shape and charge of the original SiPM signal but allows an effective suppression of baseline fluctuations due to dark counts. This is particularly important for timing measurements.

Ordering Information

ASD-EP-EB-PZ	Evaluation board with low gain output (positive output polarity) and differential output (negative output polarity).

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_A	Supply Voltage Range (V_{DD} - V_{SS})	4.5	12	V
S_{IN}	Common Mode Input Voltage	V_{SS} -0.7	V_{DD} + 0.7	V
T_A	Operating Temperature Range	-20	+60	°C
T_S	Storage Temperature	-10	+80	°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

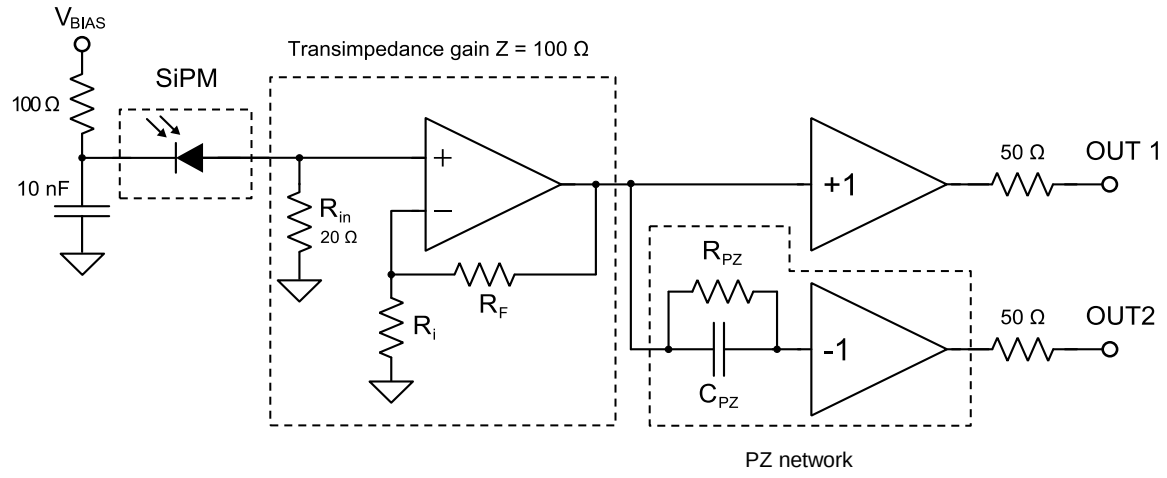
Specifications

At T_A = 25°C, V_{DD} = +5 V, V_{SS} = -5 V

Symbol	Parameter	Value	Unit
Z	Non-Inverting Stage Transimpedance Gain	100	Ω
G_1	OUT 1 Total Transimpedence(1)	50	Ω
G_2	OUT 2 Total Transimpedence(1)	n.a	-
R_{PZ}	Pole-Zero Resistance	22	k Ω
C_{PZ}	Pole-Zero Capacitance	10	pF
Z_{OUT}	Output Impedance(2)	50	Ω
I_{SS}	Supply Current	(typ.) 50	mA

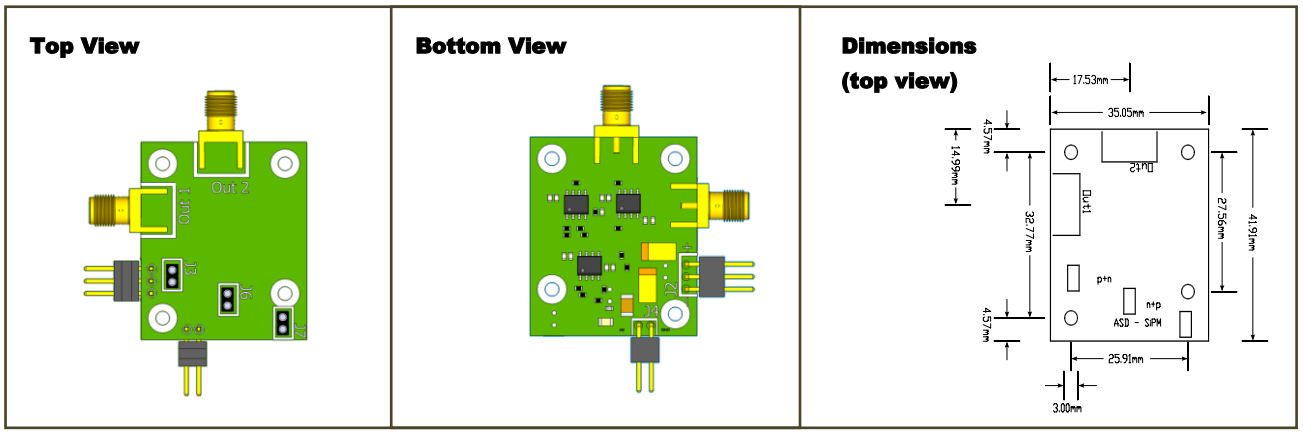
(1) Including Z, terminated on 50 Ω load

Block Diagram



ASD-EP-EB-PZ Schematic

Layout and dimensions



SiPM connections

The J6 pin header, located on the front side of the Evaluation Board, receives the anode and cathode terminals of the SiPM to be tested.

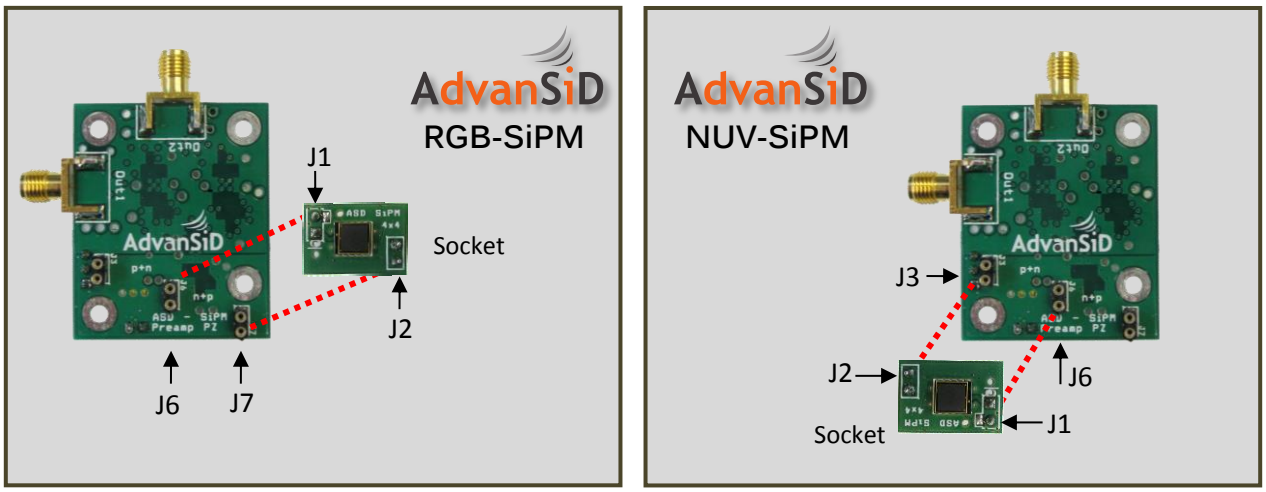
SiPMs in metal can (TO package)

The pins of metal cans can be directly inserted into J6, according to the pin-out reported on the SiPM datasheet and the Evaluation board pin-out scheme reported in this datasheet.

CSP SiPMs

CSP SiPMs connect to the evaluation board through the **AdvanSiD SiPM Sockets** available for 1x1, 3x3, 4x4 mm^2 RGB and NUV CSP SiPMs.

The SiPM Sockets insert into the AdvanSiD Evaluation Board according to the SiPM type that is carried:
Sockets with **RGB-SiPM:** J1 (Socket) into J6 (Evaluation Board); J2 (Socket) into J7 (Evaluation Board).
Sockets with **NUV-SiPM:** J1 (Socket) into J6 (Evaluation Board); J2 (Socket) into J3 (Evaluation Board).



Pin header J3 and J7 are not electrically active; they serves as mechanical support for the socket.

Pin-out

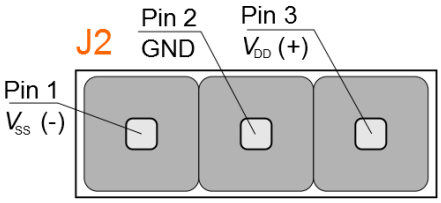
A. Amplifier Power Supply (dual power supply required)

Connector J2:

Pin 1: V_{SS}

Pin 2: GND

Pin 3: V_{DD}



Typical configuration:

V_{DD} = +5 V

V_{SS} = -5 V

Recommendations:

(V_{DD} - V_{SS}) = 10 V

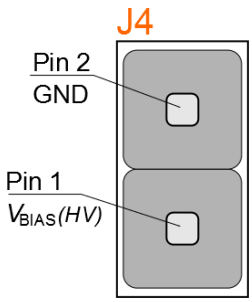
Power supply capability: >100 mA

B. SiPM Power Supply (for SiPM biasing)

Connector J4:

Pin 1 = V_{BIAS}

Pin 2 = GND



Refer to the SiPM datasheet for the specific device breakdown voltage.

Example:

$|V_{BREAKDOWN}|$ = 28 V (from SiPM datasheet)

$V_{OVERVOLTAGE}$ = 4 V (AdvanSiD SiPMs operate with 2 to 7 V overvoltage)

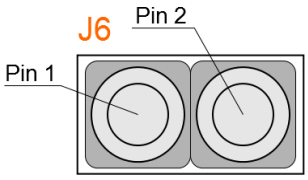
➔ V_{BIAS} = +32 V (Since it is applied in reverse mode, V_{BIAS} must be positive)

C. Input signal (SiPM anode and cathode)

Socket J6:

Pin 1 = SiPM Anode

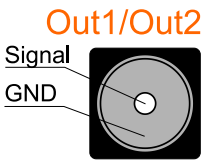
Pin 2 = SiPM Cathode



Note: Socket J6 can host metallic TO packages or the AdvanSiD socket.
Refer to the specific device datasheet for SiPM pin-out.

D. Output

SMA connectors



Note: Out1 and Out2 should be terminated with 50 Ω load for output impedance matching.